WHAT IS CLAIMED IS:

1. A method of isolating a trench, comprising:

forming a first trench and a second trench in a first region and a second region of a semiconductor substrate, respectively;

forming a lower isolation pattern to fill a lower region of the first trench; and

forming an upper isolation pattern to fill an upper region of the first trench and the second trench.

2. The method as claimed in claim 1, wherein the second trench is formed to be wider than the first trench.

3. The method as claimed in claim 1, wherein the first and second regions are a cell array region and a peripheral circuit region, respectively.

4. The method as claimed in claim 1, wherein forming the first and second trenches comprises:

forming a pad oxide pattern and a polish stop pattern which are sequentially stacked on the semiconductor substrate; and

etching the semiconductor substrate using the polish stop pattern as an etch mask.

5. The method as claimed in claim 1, wherein forming the lower isolation pattern comprises:

forming a lower isolation layer on an entire surface of the semiconductor substrate where the first and second trenches are formed;

forming a photoresist pattern on the first region of the semiconductor substrate having the lower isolation layer formed thereon, leaving the second region exposed;

etching the lower isolation layer in the second region using the photoresist pattern as an etch mask to expose at least an upper sidewall of the second trench;

removing the photoresist pattern; and

etching the lower isolation layer remaining on a resultant structure where the photoresist pattern is removed, to expose an upper sidewall of the first trench and simultaneously to form a lower isolation pattern for filling a lower region of the first trench.

6. The method as claimed in claim 5, wherein the lower isolation layer is formed of a spin on glass (SOG) layer.

7. The method as claimed in claim 5, wherein the etching of the lower isolation layer is performed using a dry etch, a wet etch, or a mixture of both.

8. The method as claimed in claim 7, wherein the etching of the lower isolation layer is performed using a wet etch including a fluoric acid as an etchant.

9. The method as claimed in claim 1, wherein the forming of the lower isolation pattern comprises:

forming a lower isolation layer on an entire surface of the semiconductor substrate where the first and second trenches are formed;

etching the lower isolation layer to form a lower isolation pattern in a lower region of the first trench;

forming a photoresist pattern on the first region of the semiconductor substrate having the lower isolation pattern formed thereon, leaving the second region exposed;

removing the lower isolation layer remaining in the second region using the photoresist pattern as an etch mask; and

removing the photoresist pattern.

10. The method as claimed in claim 9, wherein the lower isolation layer is formed of an SOG layer.

11. The method as claimed in claim 9, wherein etching the lower isolation layer is performed using a wet etch, a dry etch or a mixture of both.

12. The method as claimed in claim 1, wherein forming the upper isolation pattern comprises:

forming an upper isolation layer on an entire surface of the semiconductor substrate that results after forming the lower isolation pattern; and

planarizing the upper isolation layer to expose a top surface of the semiconductor substrate.

13. The method as claimed in claim 12, wherein planarizing the upper isolation layer is performed using a chemical mechanical polishing (CMP) process.

14. The method as claimed in claim 1, after forming the first and second trenches, further comprising forming a nitride liner on the entire surface of the semiconductor substrate comprising the first and second trenches.

15. The method as claimed in claim 14, wherein the nitride liner is formed of a low-pressure chemical vapor deposition (LPCVD) silicon nitride layer.

16. The method as claimed in claim 15, wherein the nitride liner is conformally formed to a thickness of from about 30 to 140 Å.

17. The method as claimed in claim 1, wherein the upper isolation pattern is formed of at least one of a high-density plasma (HDP) oxide layer and a USG layer.

18. The method as claimed in claim 17, wherein when the upper isolation pattern is formed of an HDP oxide layer, an LPCVD oxide layer is formed on the substrate including the nitride liner before forming the HDP oxide layer.

19. The method as claimed in claim 18, wherein the LPCVD oxide layer is formed to a thickness of about 100 Å.

20. The method as claimed in claim 1, after forming the lower isolation pattern, further comprising performing a thermal oxidizing process to densify the lower isolation pattern.

21. The method as claimed in claim 20, wherein the thermal oxidizing process is a curing process.

22. The method as claimed in claim 21, wherein the curing process uses oxygen gas or deionized water.

23. A structure of trench isolation, comprising:

a first trench and a second trench that are formed in a first region and a second region of a semiconductor substrate, respectively;

a lower isolation pattern filling a lower region of the first trench while exposing an upper sidewall of the first trench; and

an upper isolation pattern filling the second trench and an upper region of the first trench.

24. The structure as claimed in claim 23, further comprising a nitride liner pattern to cover inner walls of the first and second trenches.

25. The structure as claimed in claim 24, wherein the nitride liner is silicon nitride.

26. The structure as claimed in claim 25, wherein the nitride liner is formed by low pressure chemical vapor deposition (LPCVD).

27. The structure as claimed in claim 25, wherein the nitride liner is formed to a thickness of about 30 to 140 Å.

28. The structure as claimed in claim 23, wherein the lower isolation pattern is formed of an SOG layer.

29. The structure as claimed in claim 23, wherein the upper isolation pattern is formed of at least one of an HDP oxide layer and a USG layer.

30. The structure as claimed in claim 29, wherein when the upper isolation pattern is formed of an HDP oxide layer, an LPCVD oxide layer is formed on the substrate including the nitride liner before forming the HDP oxide layer.

31. The structure as claimed in claim 30, wherein the LPCVD oxide layer is formed to a thickness of about 100 Å.